In the Claims:

1 – 12. (canceled)

13. (new) A process of testing a semiconductor wafer comprising:

a. providing a semiconductor wafer with a scribe-line region;

b. forming a multiple test structures in the scribe-line region;

c. forming a test selector structure in the scribe-line region communicable to the multiple test structures;

d. forming two probe pads in the scribe-line region communicable to the multiple test structures and the test selector structure;

e. applying a voltage signal between the two probe pads and the selector structure to select one of the multiple test structures and to cause a electrical stimulus to be applied to the selected test structure to produce a response; and

f. measuring the response at the two probe pads.

14. (new) The process of claim 13, wherein the selecting one of the multiple test structures is accomplished by varying the magnitude of the voltage signal.

15. (new) The process of claim 13, wherein the selecting one of the multiple test structures is accomplished by varying the magnitude and the duration of the voltage signal.

16. (new) The process of claim 13, wherein the voltage signal comprises a DC voltage.

17. (new) The process of claim 13, wherein the selector structure comprises a state machine.

18. (new) The process of claim 13, wherein the selector structure comprises logic gates.

19. (new) The process of claim 13, wherein the selector structure comprises CMOS transistors of various sizes.

20. (new) A semiconductor device comprising:

    a. semiconductor wafer with a scribe-line region;

    b. a multiple test structures in the scribe-line region;

    c. a test selector structure in the scribe-line region communicable to the multiple test structures;

    d. two probe pads in the scribe-line region communicable to the multiple test structures and the test selector structure;

    e. the device adapted to receive a voltage signal between the two probe pads and the selector structure to select one of the multiple test structures and to cause a electrical stimulus to be applied to the selected test structure to produce a response; and

    f. the response measurable at the two probe pads.

21. (new) The device of claim 20 wherein the selector structure is a multiplexer adapted to select only one test structure at a given voltage signal.

22. (new) The device of claim 20, wherein the selecting one of the multiple test structures is accomplished by varying the magnitude and the duration of the voltage signal.

23. (new) The device of claim 20, wherein the selecting depends on the magnitude of the voltage signal.

24. (new) The device of claim 20, wherein the selecting depends on the magnitude and the duration of the voltage signal.

25. (new) The device of claim 20, wherein the selector structure comprises CMOS transistors of various sizes.

26. (new) The device of claim 20, wherein the selector structure comprises logic gates.